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Art Unit: 2127
Amendment dated June 15, 2004
Reply to Office Action March 16, 2004

<u>Amendments to the Claims:</u>

Claim 1 (currently amended):   A method of processing communication channels, comprising:

for each of a plurality of channels:

undertaking a given channel processing task for a given channel with one processor of a plurality of processors, said one processor ~~optimised~~ optimized for said given channel processing task;

storing instance data for said given channel processing task in a memory which may be associated with any one of said plurality of processors such that said instance data is associated with said one processor;

when said given channel processing task for said given channel changes to a new channel processing task for which said one processor is not ~~optimised~~ optimized,

moving processing of said given channel to a different one of said plurality of processors, said different one of said processors being ~~optimised~~ optimized for said new channel processing task, and

changing association of said stored given channel instance data to an association with said different processor.

Claim 2 (original): The method of claim 1 wherein said given channel instance data comprises a history buffer storing historical data samples for a signal on said given channel.

Claim 3 (original): The method of claim 1 wherein said given channel instance data comprises a jitter buffer.

Claim 4 (currently amended): The method of claim 1 wherein said moving comprises consulting a table for a processor ~~optimised~~ optimized to said new channel processing task.

Claim 5 (original): The method of claim 1 wherein said memory is a multiplexed memory.

Claim 6 (currently amended): The method of claim 1 further comprising, where said one processor is ~~optimised~~ optimized for said new channel processing task, undertaking said new channel processing task for said given channel at said one processor.

Claim 7 (original): The method of claim 6 further comprising keeping a table with an identification of available ones of said plurality of processors and an identification of processing tasks handled by said available ones of said plurality of processors.

Claim 8 (original): The method of claim 5 wherein said changing association comprises overwriting a latch holding an address of said one processor with an address of said different processor.

Claim 9 (currently amended): A method of processing communication channels comprising:

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at each of a plurality of processors:

undertaking a channel processing task using a multiplexed memory having a plurality of channel memory partitions, each channel memory partition for storing channel instance memory data for a given channel;

when said channel processing task changes to a new channel processing task:

referencing a table to identify a processor of said plurality of processors optimised optimized to said new channel processing task,

prompting said new task optimised optimized processor to assume processing of said channel, and

arranging for an associator to associate channel instance memory data stored in one of said channel memory partitions and associated with for said given channel with said new task optimised optimized processor.

Claim 10 (currently amended): A multiprocessor system for processing communication channels, comprising:

a plurality of processors, each optimised for at least one channel processing task and each having processor memory for storing information associating different channel processing tasks to different ones of said plurality of processors;

a multiplexed memory for storing channel processing instance data for each of said plurality of processors;

an associator for associating channel processing instance data for each channel with one of said plurality of processors;

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each processor of said plurality of processors operable to, on a channel processing task for a channel currently being processed by said each processor changing to a new task,

arrange for said associator to associate instance data for said channel with a processor optimised optimized to said new task.

Claim 11 (currently amended): The system of claim 10 further comprising a host for, on a channel processing task for a channel currently being processed by a given processor changing to a new task, sending to said given processor an indication of said processor optimised optimized to said new task.

Claim 12 (original): The system of claim 10 wherein said associator comprises a latch for channel instance data of a given channel, each said latch being latched to a given processor processing said given channel and arranged such that only said given processor may change said latch to latch to a new processor.

Claim 13 (original): The system of claim 12 wherein said associator further comprises a multiplexer mapping memory read/write requests from said given processor to instance channel data for said given channel in said shared memory.

Claim 14 (original): The system of claim 13 wherein each of said plurality of processors is a digital signal processor ("DSP").